

**Amendments to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. 1. (previously presented) A system, comprising:
  2. a backplane having a plurality of conductors;
  3. a first plurality of printed circuit boards plugged into the backplane, each one of the first printed circuit boards having a plurality of electrical contacts, each one of the electrical contacts providing an indication of an incapability of an electrical component on such one of the printed circuit boards, each one of such electrical contacts of the first plurality of printed circuit boards being electrically connected together through a corresponding one of the plurality of conductors of the backplane;
  9. circuitry connected to the plurality of conductors for converting the operating incapability indications provided by the plurality of printed circuit boards into logic signals on the plurality of conductors;
  12. a second plurality of printed circuit boards plugged into the backplane, each one of the second plurality of printed circuit boards having a decoder responsive to the logic signals on the plurality of conductors for selecting an operating characteristic for electrical components on the second plurality of printed circuit boards, such selected operating characteristic being compatible with operating characteristics of the electrical components on the first plurality of printed circuit boards.
1. 2. (original) The system recited in claim 1 wherein the operating characteristic is operating speed and wherein the decoders select the highest speed compatible with the speed capability of the electrical components on the plurality of first printed circuit boards.
1. 3. (previously presented) A system, comprising:
  2. a backplane having a plurality of conductors;

3           a first plurality of printed circuit boards plugged into the backplane, each one of the  
4        first printed circuit boards having a plurality of electrical contacts, each one of the electrical  
5        contacts providing an indication signal representative of a predetermined operating  
6        incapability of an electrical component on such one of the printed circuit boards, each one of  
7        such electrical contacts of the first plurality of printed circuit boards being electrically  
8        connected together through a corresponding one of the plurality of conductors of the  
9        backplane;

10           a second plurality of printed circuit boards plugged into the backplane, each one of  
11        the second plurality of printed circuit boards having a decoder responsive to the incapability  
12        indication signal on the plurality of conductors for selecting an operating characteristic for  
13        electrical components on the second plurality of printed circuit boards, such selected  
14        operating characteristic being compatible with operating characteristics of the electrical  
15        components on the first plurality of printed circuit boards.

1        4. (original) The system recited in claim 3 wherein the operating characteristic is operating  
2        speed and wherein the decoders select the highest speed compatible with the speed  
3        capability of the electrical components on the plurality of first printed circuit boards.

1        5. (previously presented) A system, comprising:

2           a backplane having a plurality of conductors;  
3           a first plurality of printed circuit boards plugged into the backplane, each one of the  
4        first printed circuit boards having a plurality of electrical contacts, each one of the electrical  
5        contacts providing an indication of a predetermined speed incapability of an electrical  
6        component on such one of the printed circuit boards, each one of such electrical contacts of  
7        the first plurality of printed circuit boards being electrically connected together through a  
8        corresponding one of the plurality of conductors of the backplane;

9           circuitry connected to the plurality of conductors for converting the operating speed  
10        incapability indications provided by the plurality of printed circuit boards into logic signals  
11        for the plurality of printed circuit boards;

12           a second plurality of printed circuit boards plugged into the backplane, each one of  
13        the second plurality of printed circuit boards having:

an electrical component; and

a source of a plurality of clock signals, each one of the plurality of clock

signals having a different rate;

a decoder for coupling one of the plurality of clock signals to the electrical connection on such one of the second plurality of printed circuit boards selectively in accordance with the provided logic signals; and

wherein the decoders of the second plurality of printed circuit boards couple to electrical components thereon the one of the plurality of clock signals having a incompatible with operating speeds of the electrical components on the first plurality of printed circuit boards.

- 1 6. (original) The system recited in claim 5 wherein the circuitry provides a wired-NOR
- 2 configuration.
- 1 7. (original) The system recited in claim 5 wherein each one of the plurality of contacts is
- 2 connected to ground potential when such contact provides an indication of operating
- 3 speed incapability; otherwise such contact is open circuited.
- 1 8. (original) The system recited in claim 7 wherein the circuitry provides a wired-NOR
- 2 configuration.
- 1 9. (original) The system recited in claim 5 wherein the decoders select as the rate a rate
- 2 compatible with operating speeds of the electrical components on the first plurality of
- 3 printed circuit boards the one of the plurality of clock signals having the highest rate
- 4 compatible with the speed capability of the electrical components on the plurality of first
- 5 printed circuit boards.
- 1 10. (previously presented) A system, comprising:
  - 2 a backplane having a plurality of conductors;
  - 3 a plurality of resistors, each one connected between a corresponding one of the
  - 4 plurality of conductors and a voltage source;

5        a first plurality of printed circuit boards plugged into the backplane, each one of the  
6        first printed circuit boards having a plurality of electrical contacts, each one of the electrical  
7        contacts of the first plurality of printed circuit boards being connected to a corresponding one  
8        of the plurality of conductors, each one of such contacts being connected to either ground or  
9        to an open circuit, connection to ground providing an indication of an operating speed  
10      incapability of an electrical component on such one of the first printed circuit boards;

11                wherein the contact connected to ground provides a first logic state on the one of the  
12        plurality of conductors connected thereto when such contact is connected to ground and  
13        provides a second logic state on the one of the plurality of conductors connected thereto when  
14        such contact is connected to an open circuit;

15        a second plurality of printed circuit boards plugged into the backplane, each one  
16        thereof having:

17                an electrical component; and

18                a source of a plurality of clock signals, each one of the plurality of clock  
19        signals having a different rate;

20                a decoder for coupling one of the plurality of clock signals to the electrical  
21        component on such one of the second plurality of printed circuit boards selectively in  
22        accordance with the provided logic states; and

23                wherein the decoders of the second plurality of printed circuit boards couple to  
24        the electrical components thereon the one of the plurality of clock signals having a  
25        rate compatible with operating speeds of the electrical components on the first  
26        plurality of printed circuit boards.

1        11. (original) The system recited in claim 10 wherein the decoders selects as the rate a rate  
2        compatible with operating speeds of the electrical components on the first plurality of  
3        printed circuit boards the one of the plurality of clock signals having the highest rate  
4        compatible with the speed capability of the electrical components on the plurality of first  
5        printed circuit boards.

1        12. (previously presented) A system comprising:  
2                a backplane having a plurality of conductors;

3 a plurality of printed circuit boards plugged into the backplane, each one of the  
4 printed circuit boards having a plurality of electrical contacts, each one of the electrical  
5 contacts providing an indication of a predetermined operating incapability of an electrical  
6 component on such one of the printed circuit boards, each one of such electrical contacts of  
7 the plurality of printed circuit boards being electrically connected together through a  
8 corresponding one of the plurality of conductors of the backplane;

9 circuitry connected to the plurality of conductors for converting the operating  
10 incapability indications provided by the plurality of printed circuit boards into logic signals  
11 for the plurality of printed circuit boards.

1 13. (original) The system recited in claim 12 wherein the operating incapability is operating  
2 speed.

1 Cancel claim 14.

1 Cancel claim 15.

1 Cancel claim 16.

1 Cancel claim 17.

1 18. (currently amended) A method for operating a system, comprising:  
2 providing a backplane system comprising:  
3 a plurality of printed circuit ~~broads~~ boards each one having an electrical  
4 component thereon; and  
5 a backplane having plugged therein the plurality of printed circuit boards  
6 for producing a signal indicative of a speed compatibility of the electrical  
7 components;  
8 plugging an additional printed circuit ~~broad~~ board having an electrical component  
9 thereon into the provided backplane, the electrical component on such additional printed

10 circuit board being incompatible with the speed of the electrical components on the plurality  
11 of printed circuit boards;

12 an electrical circuit for electrically inhibiting the electrical coupling of the electrical  
13 component on the additional printed circuit board from the electrical components of the  
14 plurality of printed circuit boards.

1 19. (previously presented) A method comprising:

2 providing a backplane having a plurality of conductors with a plurality of printed  
3 circuit boards plugged into the backplane, each one of the printed circuit boards having a  
4 plurality of electrical contacts, each one of the electrical contacts providing an indication of a  
5 predetermined operating incapability of an electrical component on such one of the printed  
6 circuit boards, each one of such electrical contacts of the plurality of printed circuit boards  
7 being electrically connected together through a corresponding one of the plurality of  
8 conductors of the backplane; and

9 converting the operating incapability indications provided by the plurality of printed  
10 circuit boards into logic signals for the plurality of printed circuit boards.

1 20. (original) The method recited in claim 19 wherein the operating incompatibility is  
2 operating speed.

21. (original) The method recited in claim 19 wherein the operating incompatibility is  
operating protocol.